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MILESTONE REPORT

UPGRADE OF IRRAD BPM DAQ

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Abstract:

The Beam quality is of the utmost importance in the operation of the CERN proton irradiation facility (IRRAD). Dedicated Beam Profile Monitor (BPM) sensors based on the Secondary Electron Emission (SEE) process were developed and recently significantly improved thanks to a new manufacturing technology based on microfabrication of metal nano-layers. Today, to be able to exploit all features of these new BPMs, the DAQ technology, as well as the handling and display of the BPM data need also to be substantially improved. This report describes the upgrades performed on the IRRAD BPM DAQ to cope with the increasing sensor sensitivity, the new timing performance required to monitor the IRRAD beams, as well as to enable the facility's operator and user teams to profit of these new and advanced features. This development will also facilitate the use of the BPM system in other EU irradiation facilities for the monitoring of their various (in type and energy) particle beams and, in particular, the most challenging low-energy beams.

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1. INTRODUCTION

The beam quality is of utmost importance in the operation of an irradiation facility. For the proton irradiation facility at CERN (IRRAD), a dedicated Beam Profile Monitor (BPM) sensor was developed and recently significantly improved thanks to a new manufacturing technology based on microfabrication of metal nano-layers.

In particular, the new BPM sensor features a minimal particle interaction (non-invasive) and an improved radiation hardness (lifetime reliability). Today, to be able to exploit all features of these new BPMs, the DAQ technology as well as the handling and display of the BPM data need also to be substantially improved. In particular, the existing DAQ technology employed for the BPM sensors readout needed to be upgraded in order to cope with increasing sensitivity, timing performance so as to enable the final users to profit from these new and advanced features.

Both the data handling techniques and the improvement in the readout DAQ electronics detailed in this report for the BPM instrument can be later adopted by the other EU irradiation facilities for the monitoring of the available various (species and energies) particle beams.

In this document we describe the complete development process of the new IRRAD BPM DAQ, including the design and testing of the components, providing a general overview of the functionalities of the product and its performance.

1.1. PROJECT REQUIREMENTS

The main requirements for the design of the new IRRAD-BPM DAQ were the possibility to measure currents in the 1-100's nA range (matching the dynamic range of the new BPM sensors) with a variable sampling rate reaching the 1 ms range (to be compared with the fixed sampling rate of the former DAQ system used in IRRAD of 20 ms) [1]. The new system has also to be able to acquire and process signals from several IRRAD BPM devices, each one consisting of a set of 40 channels.

2. PROJECT CHOICES

In this section all the choices made for the design of the new system will be analysed. The following sections describe some key components as well as the definition of the global project architecture.

2.1. TEXAS INSTRUMENTS' DDC232

The DDC232 [2] is a 20-bit, 32-channel, current input Analog-to-Digital (A/D) converter. Thanks to the combination of current-to-voltage and A/D conversion the acquisition of 32 separate low-level current output devices is possible, for e.g., the pads of the BPM described above. Some of the features are listed below:

- Low Power: 7 mW / channel
- Adjustable Full-Scale Range (FSR)
- Daisy-Chainable Serial Interface
- Low Noise: 5.3ppm of FSR

The Block Diagram is shown in *Figure 1*. On the left side is possible to see 32 identical input channels which are Dual Switched Integrators and perform the function of current-to-voltage integration followed by a Delta Sigma ADC. On each input there are two integrators to offer a continuous integration in time. The outputs of the 64 integrators are switched to 16 delta-sigma converters via multiplexers. The basic principle is to digitize the input from one side and to use the other 32 integrators to integrate the next input at the same time. Everything is controlled by a system clock

(CLK) and every result is stored in a serial output shift register, through the DOUT pin which gives 20-bit words at every rising of a readout clock signal (DCLK).

2.1.1. BASIC INTEGRATION CYCLE

The DDC232 has 32 channels, but each channel executes a dual integration process. In this subsection we will describe only one integrator, since the second one is working following the same diagram. The input stage is an operation amplifier configured as an integrator.

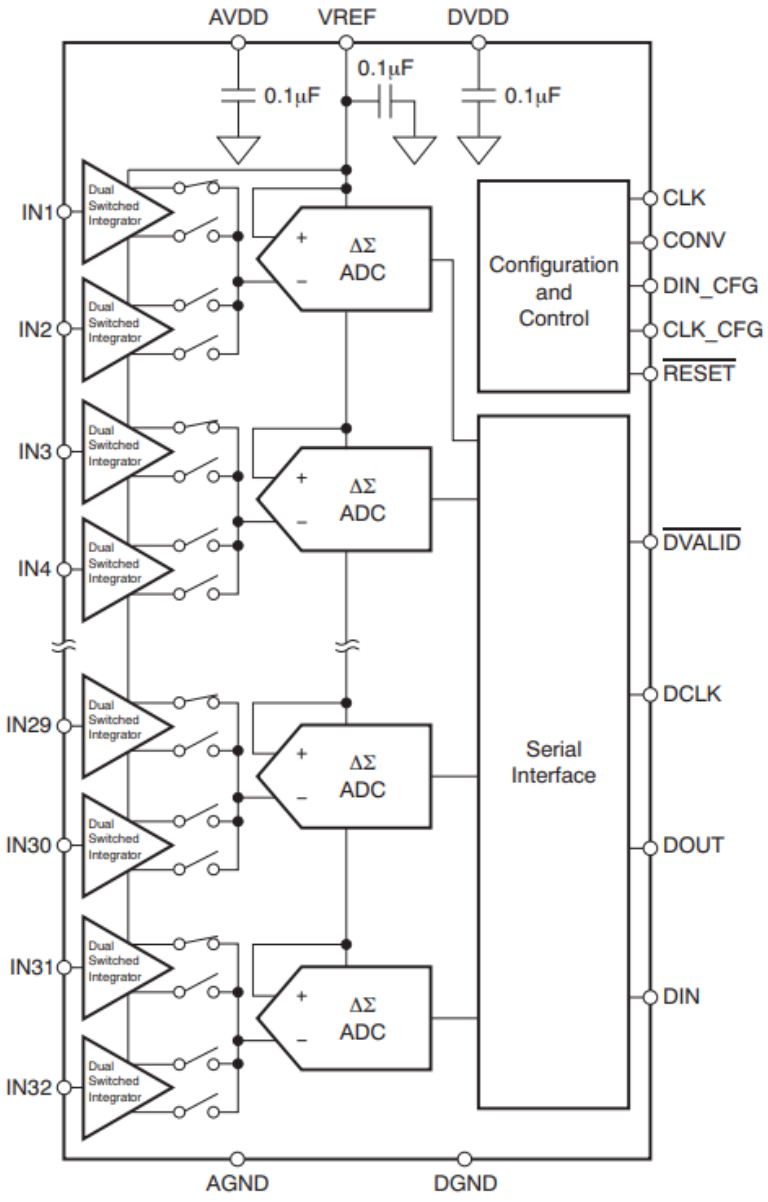

Figure 1 - DDC232 Block Diagram

According to what was said before, it is necessary to perform the charge amplification and for this reason the OP Amp is equipped with a feedback capacitor network and several switches that implement the integration cycle. The capacitor network is designed to allow the configuration of the range of the DDC232: the range control bits change the capacitor value for all the integrators. Consequently, all inputs and both sides of each input will always have the same full-scale range. For other features about DDC232 architecture are given in [2].

2.1.2. DIGITAL INTERFACE

As shown in *Figure 1*, the DDC232 has a digital interface called Configuration and Control that produces a serial output. The main pins of this interface are:

- Data Clock – DCLK
- Valid Data - !DVALID (the "!" indicates that this signal is active-low)
- Data Output – DOUT
- Data Input – DIN
- Reset – RST

CLK and DCLK frequencies are not required to be the same since the integration and conversion process are independent. The DIN pin is not used since it's required only when multiple converters are cascaded. For this reason, it is put at a Digital Ground (DGND). Regarding the clock signal, the system clock (CLK) is supplied to CLK, and the data clock is supplied to DCLK. Not all data coming out from the DOUT pin are valid data to be read, for this reason the !DVALID signal indicates that data are ready. Notice that the pin is active low, which means that readout can start only when the !DVALID pin goes low. Regarding the CONV signal, when this goes low, the integration finishes on side A and starts on side B. Immediately after CONV goes low, A/D Conversion starts first on the odd channels and later on the even channels. After both conversions, data are ready to be read, so the !DVALID pin goes low for as long as necessary to read data.

2.2. PJRC TEENSY 4.1

The Teensy 4.1 [3] (see *Figure 2*) is a powerful microcontroller board designed for high-performance applications, created by PJRC. The board has the following features:

- **Microcontroller**: The Teensy 4.1 is based on the NXP i.MX RT1062 processor, which has an ARM Cortex-M7 core running at 600 MHz; it also features a floating-point unit (FPU) and a memory management unit (MMU), which enable faster and more efficient processing of data.
- **Memory**: The Teensy 4.1 has 1 MB of Flash memory for program storage and 1 MB (512 Kb tightly coupled) of RAM. Additionally, it has 4 MB of external Flash memory that can be used for larger programs or data storage and 8 MB of ext. RAM.
- **Input/Output**: It has a total of 55 I/O pins, which can be used for digital input/output, analog input, PWM output and more. It also features 8 hardware serial ports, 3 I2C, 3 SPI ports and 3 CAN Bus (1 with CAN FD) ports, which enable communication with other devices.
- **Communication**: The Teensy 4.1 supports a variety of communication protocols, including USB 2.0, Ethernet and CAN bus. It also features a built-in MicroSD card reader, which can be used for data storage.
- **Power**: It can be powered through a USB connection or an external power source (5V). It also features a built-in voltage regulator which reduces the 5V VUSB/VIN power to 3.3V.
- **Size**: It offers a 61mm x 18mm board, making it compact and easy to integrate into projects.

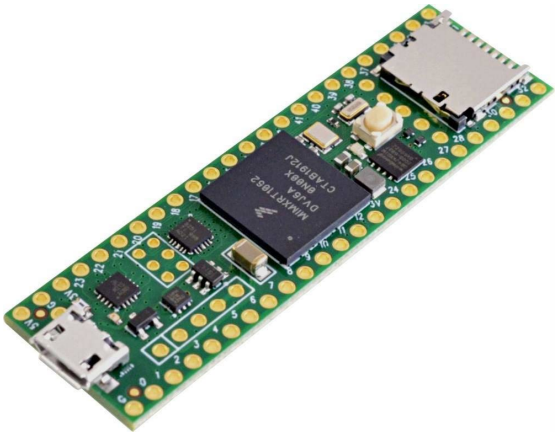

Figure 2 -Microcontroller board: Teensy 4.1

The Teensy 4.1 was selected as the preferred microcontroller to acquire data from the DDC232 for several reasons. It is well-suited for high data transfer rates due to its powerful ARM Cortex-M7 processor. This allows for quick and efficient data acquisition from the Texas Instruments IC. Moreover, the fast-processing speed of the Teensy 4.1 ensures that the data is acquired and processed in a timely manner, without any significant delay. Compatibility with the DDC232 is excellent, making the Teensy 4.1 easy to be integrated into the project and ensuring a seamless and reliable data acquisition process. Of course, the wide range of features and functionalities, such as GPIO pins, analog inputs and serial communication ports, can be used to interface with various sensors and devices.

3. SYSTEM ARCHITECTURE

The system consists of several Printed Circuit Boards (PCBs), including a large motherboard that serves as the central hub, five smaller interposer boards that will be placed as *shields*, and a panel board that functions as the user interface, as shown in the schematic of *Figure 3*.

Each interposer board is equipped with a DDC232, which provides analog-to-digital conversion and signal conditioning for the BPM sensor. The choice of 5 interposers has been made to achieve a total of 160 channels and thus be able to acquire the signal of 4 IRRAD-BPM sensors with a unique DAQ system. Since these components are expensive and difficult to manage due to low pitch, using interposer boards allows for easy replacement in case of a malfunction, without the need to replace the entire motherboard or perform complex soldering operations. This approach simplifies maintenance and reduces the cost of repairing the system.

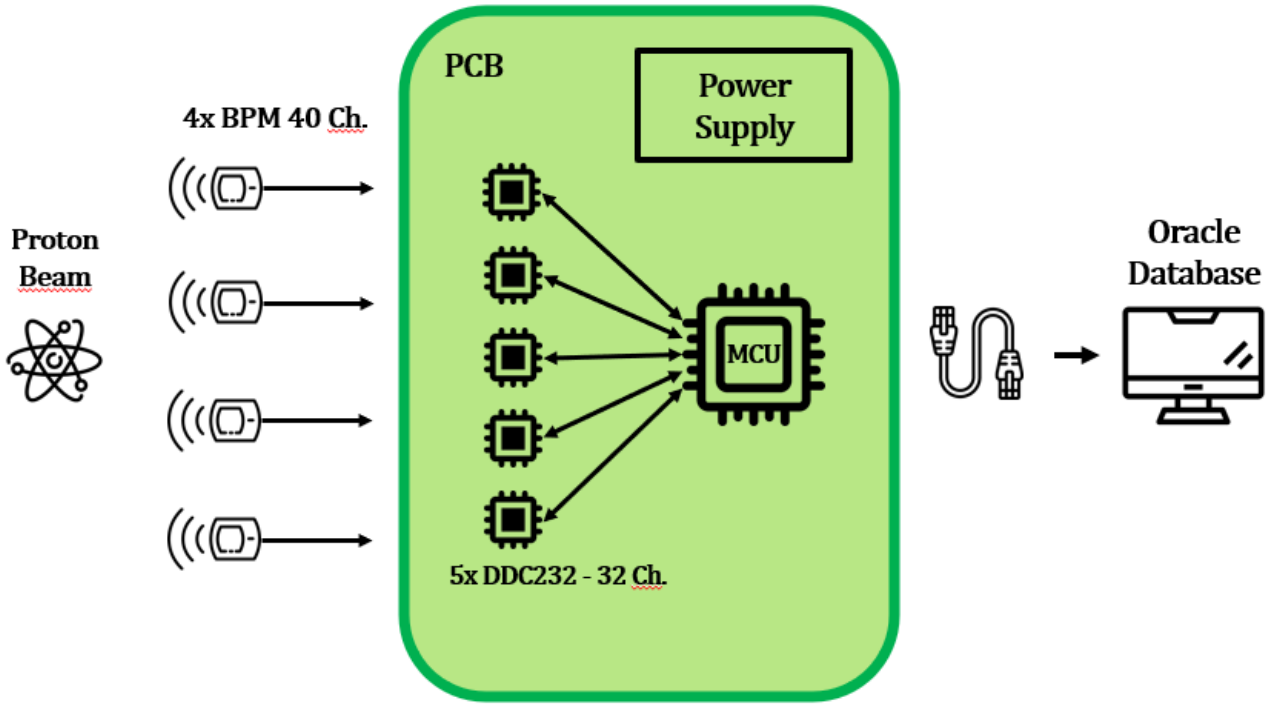

Figure 3 - System Architecture

The motherboard serves as the central hub of the front-end interface for the BPM sensor. It includes several critical components, such as a microcontroller, power supply circuits, clock generation circuits, and various connectors. The microcontroller used in this system, as seen before, is the Teensy 4.1 which is responsible for acquiring the DDC232 output signals from the interposer boards and processing them to generate meaningful sensor readings. It also controls the panel board and manages the user interface, enabling the user to monitor some basic information on an OLED display and to access to some I/O ports such as LEMO® connectors to send external triggers.

In addition, the motherboard includes a Power over Ethernet (PoE) feature, which allows the system to receive power and data through a single Ethernet cable. This feature simplifies the installation and reduces the number of cables needed, making the system more compact and user-friendly.

The overall design of the system aims to provide a reliable and cost-effective solution for the BPM sensor, with a user-friendly interface for easy operation and maintenance. The use of interposer boards and a modular architecture allows for easy expansion and customization of the system, depending on the specific requirements of each application. This gives the system a large compatibility not only for IRRAD's BPM operations but also for other beam monitoring applications.

3.1. POWER CONSUMPTION

In the following table a power requirement calculation has been done. Note that some of the used electronic components listed in the table are not described in this document.

Component	Quantity	Supply Voltage [V]	Current(x4) [A]	Power (W)
DDC232CK	5	5	0.24	6
DDC232CK	5	3.3	0.032	0.528
Teensy 4.1	1	5	0.4	2
SI5351A-B-GTR	1	3.3	0.14	0.462
SN74LVC1G80	1	5	0.128	0.64
REF3140AIDBZT	1	5	0.00054	0.0027
CFM-6015V-122-145-20	2	12	0.116	1.4

According to the estimation presents in the table above, the total power consumption is calculated to be around 11W, considering that for every device a safety factor of 4 has been used.

3.1.1. POWER OVER ETHERNET (PoE)

Power over Ethernet (PoE) [4] is a technology that allows for power to be transmitted over the same Ethernet cable that carries data, which can be useful in a variety of situations, such as when power outlets are not easily accessible or when multiple devices need to be powered from a single source.

According to the tests that were carried out on the first release, one of the main reasons to adopt PoE is that the board often required a restart, and it was not always possible to do so due to the fact that the problem occurred during non-working hours or at times when the facility was not accessible. Therefore, the possibility of performing a remote power cycle makes everything more reliable and controllable.

To implement the PoE protocol on the project it was decided to purchase a ready-to-use PoE module, in this case the PEM3012C [5] produced by Infomart IT Solutions® (see *Figure 4*). The PEM3012C is a PoE Powered Device (PD) which has a complete compliance with the high-power IEEE 802.3at PoE+ standard and it is designed to extract power from CAT5 Ethernet cable when sourced by both IEEE 802.3at and IEEE 802.3af compliant Power Sourcing Equipment (PSE). It is equipped with and high efficiency DC-DC converter which provides up to 30W of power in a well-regulated, low noise and low ripple output with built-in in-rush current, overload and output short-circuit protection.

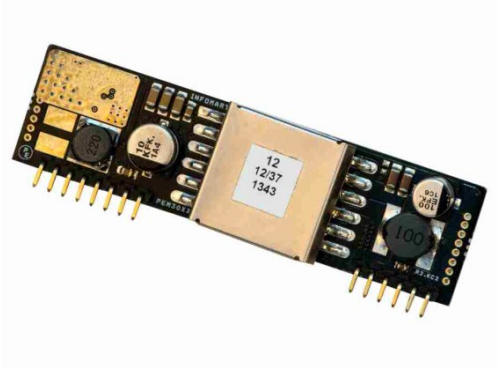

Figure 4 - PEM3012C

Some features of this product will not be used, such as the AT Detection pin, since they are not useful for this application. The AT Detection pin allows the device to understand if the Powered Device (PD) is requiring more than 15.4W to the PSE and in this case to switch from IEEE 802.3af to IEEE 802.3at protocol. According to the estimated power consumption of the system, the 15.4W protocol is more than enough to supply the circuit, so it's unnecessary to include the additional circuitry to use this feature. Switching to 30W mode is not only useless for this application, but also can make it more difficult to dissipate the generated heat. According to thermal performance profile on the datasheet, the module performances start to degrade around 55°C.

3.2. INTERPOSER BOARDS

Apart from the motherboard, the project includes five smaller interposer boards that host a single DDC232. Those boards will be placed as shields, thus interfacing to the motherboard. The choice of creating interposer boards as shields allows to place them easily and quickly, thus simplifying the assembling procedure of the motherboard and providing an easy maintenance in case of malfunction. Together with the DDC232, the interposer board hosts the Voltage Reference circuit shown in *Figure 5*. Details about the interposer board can be seen in *Figure 6*.

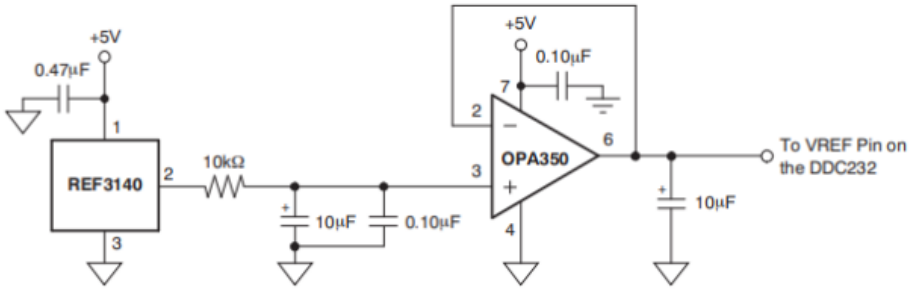

Figure 5 - DDC232 Voltage Reference Circuit

The choice to make 5 different VREF circuits, one for each interposer board, is motivated by the fact that this is a very noise sensitive circuit. Moreover, this circuit is used by the delta-sigma converters while the converter is measuring the voltage stored on the integrators after an integration cycle ends. During this sampling the external voltage reference must supply the charge needed by the delta-sigma converter. It's critical that VREF signal remains stable during the different modes of operation because the delta-sigma converter measures the voltage on the integrator with respect to VREF.

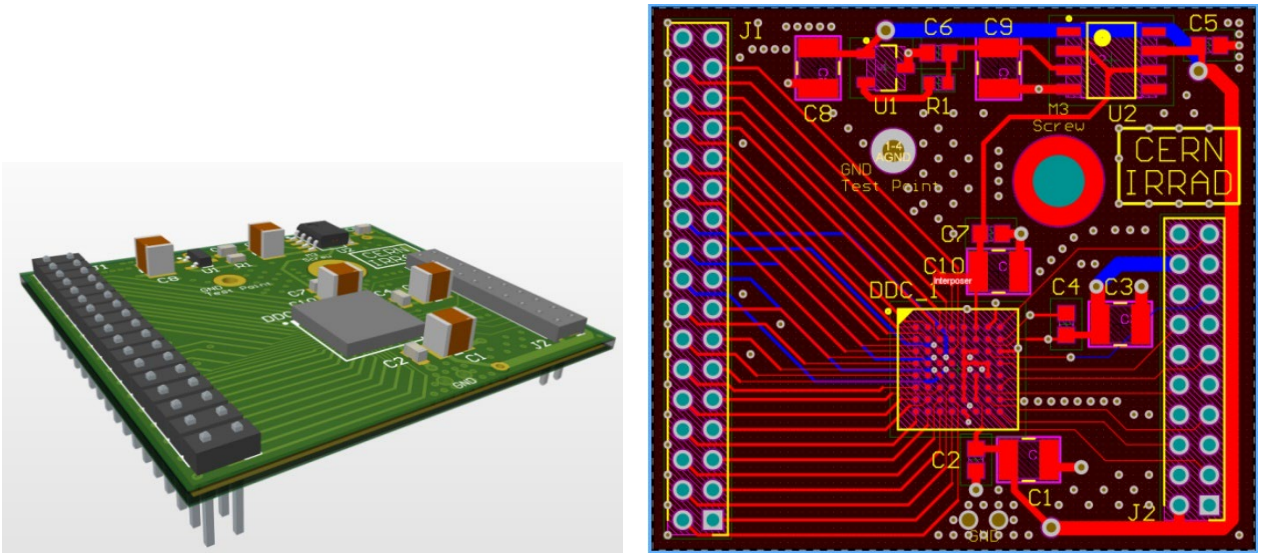

Figure 6 – Interposer Board 3D view (left) and routing (right)

4. FROM MANUFACTURING TO TROUBLESHOOTING

Figure 7 shows the final layout of the manufactured motherboard prototype, including one interposer board and an additional panel board which has been printed since the whole system is going to be mounted into a rack-mounted box, consequently creating the necessity to have a panel board including a display OLED and some I/O connections.

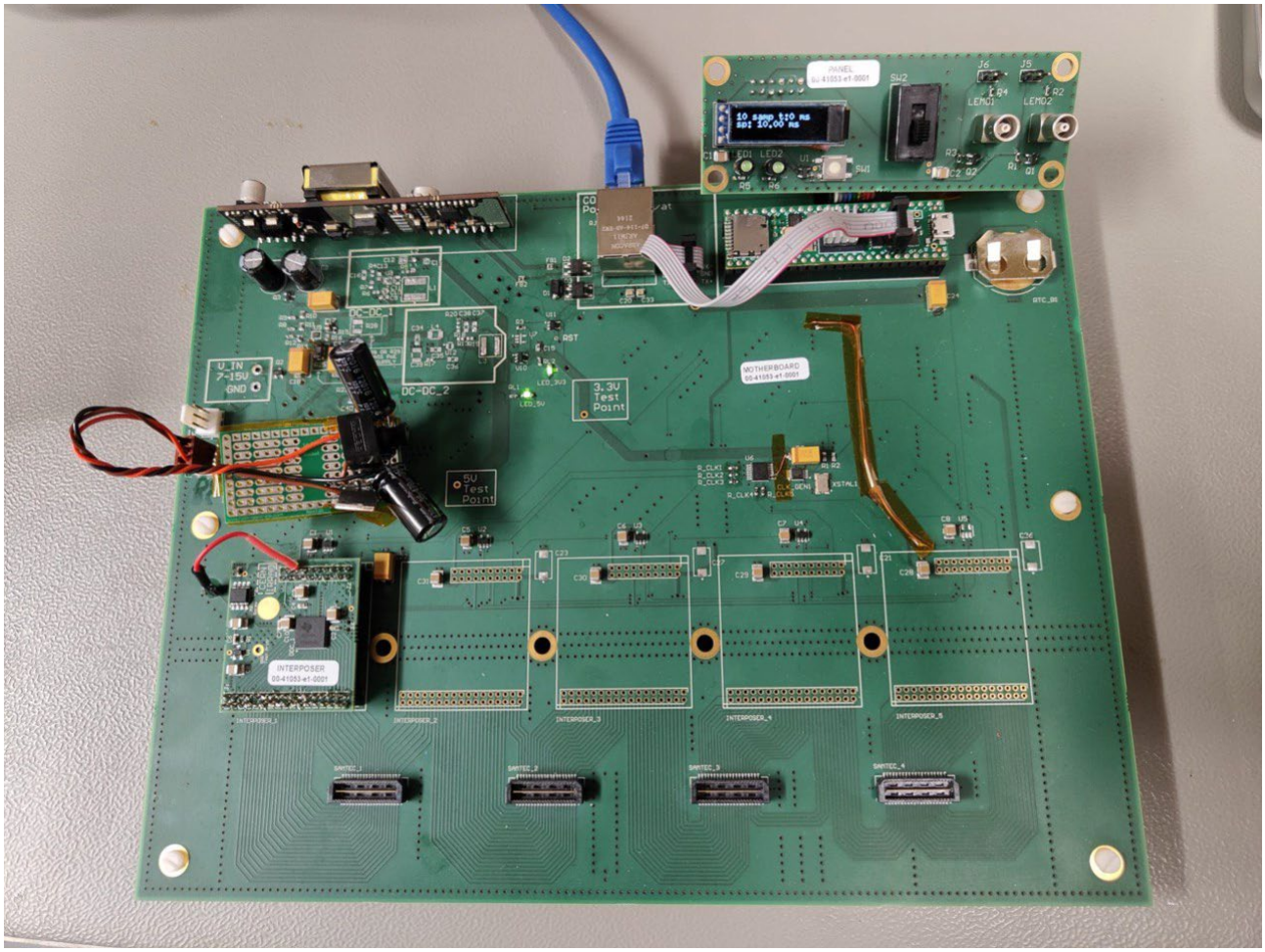

Figure 7 – Prototype of the Motherboard

Through a combination of rigorous testing methodologies and advanced diagnostic tools, the debugging process efficiently identified and rectified various challenges. However, by effectively isolating and bypassing the issues encountered, the final product demonstrated its ability to deliver each signal correctly. *Figure 7* shows the final board fully assembled and functioning, where it is possible to notice that some external wiring and components were mounted, with reference to the power supply part which provided for the scaling of the voltage from 12V to 5V. By incorporating these external components, the project showcased adaptability in overcoming obstacles and still managing to give the necessary supply voltage to all the downstream circuits.

4.1. MEASUREMENTS

The first test conducted on the prototype was about the clock generation circuit, with the aim of understanding if the integrated circuits used for the clock generation were working.

Figure 8 shows the trend of the clock signal measured downstream of each fanout buffer output using a Teledyne-LeCroy® HDO6104-MS oscilloscope. The trend of the clock signal, the duty cycle and the amplitude are consistent with what was expected. *Figure 8* also shows a measurement using cursors of the clock frequency. It is possible to see how the frequency is exactly equal to 20 MHz, in accordance with what is set in the Teensy®4.1 microcontroller firmware.

Figure 8 - Clock Measurement

Subsequently, several signals associated with the operation of the DDC232 were tested. Taking as a reference the DDC232 datasheet [2] the timing diagram of the DDC232 has been reproduced. It is possible to see in *Figure 9* the display of the CONV signal with reference to the DCLK and DOUT signals. Subsequently, *Figure 10* shows the trend of the !DVALID signal again with reference to the DCLK and DOUT signals.

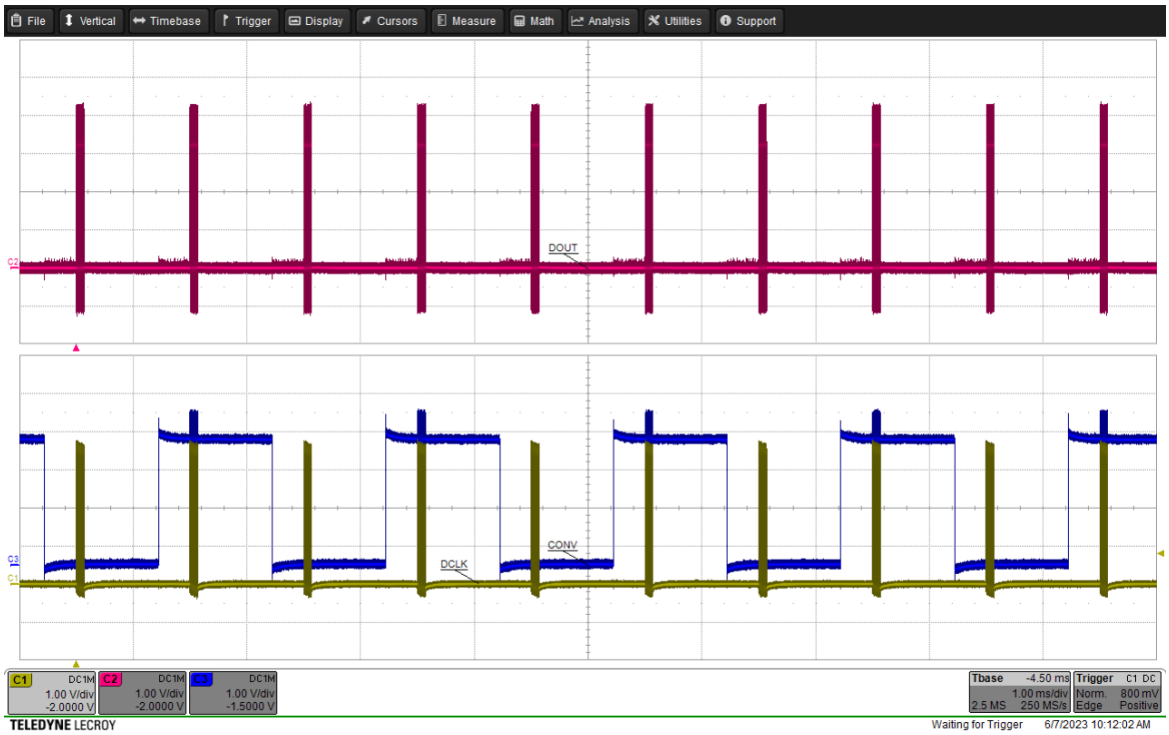

Figure 9 - DDC232 timing

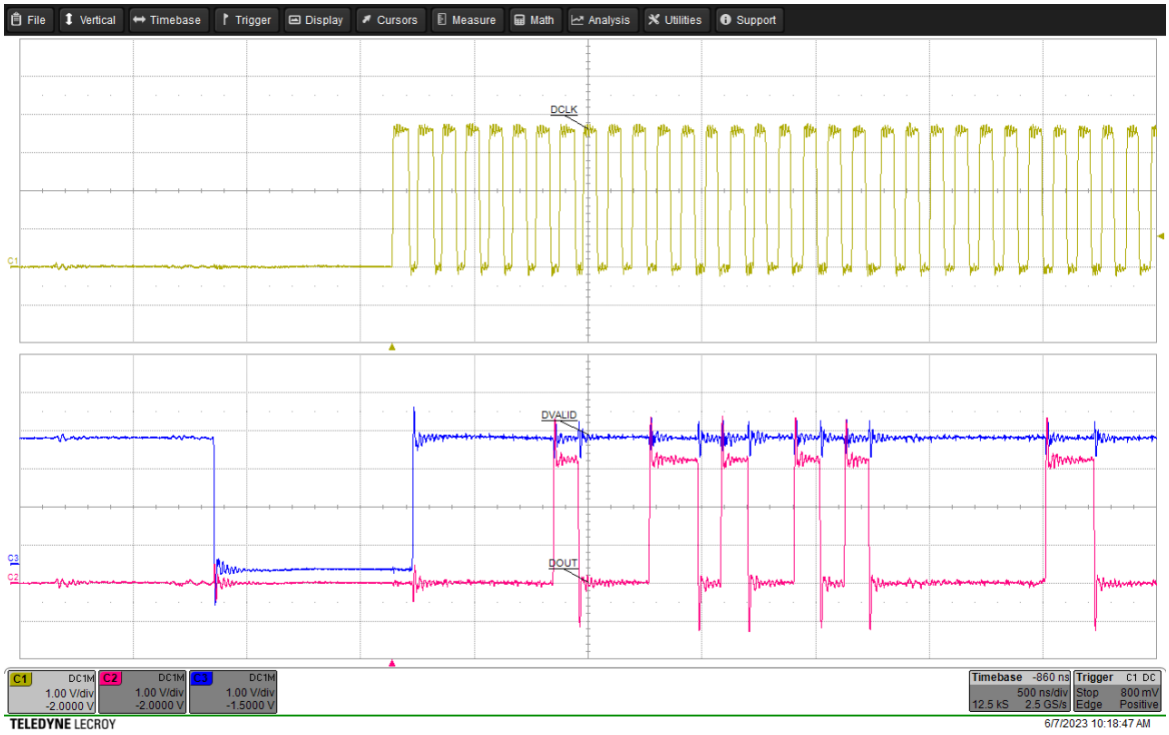

Figure 10 - DDC232 timing

4.2. TEST WITH SYNTHETIC CURRENT SIGNALS

A comprehensive test was conducted to evaluate the functionality and performance of the board which, as said before, was designed to read 40 channels (currents) for each IRRAD-BPM. These signals are available in the counting room of the IRRAD facility on a Samtec® connector. In order to apply test current signals to the PCB, a specifically designed test board equipped with 40 LEMO® connectors was used. Each connector was connected to an individual channel on the PCB, ensuring precise and separate application of the test signals as shown in *Figure 11*.

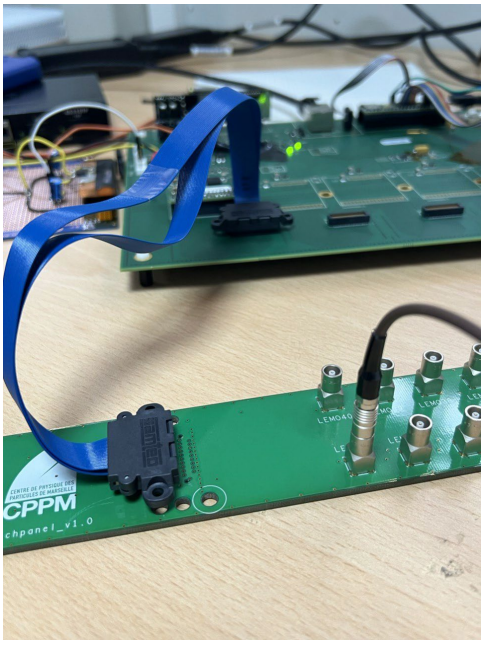

Figure 11 - Measurement Setup

The first test performed was the verification of the mapping of the connector. In particular, it was ensured that the Samtec® connector was correctly connected to the channels of the interposer board without signal interruptions or short-circuited pins.

Whereas the typical currents generated by BPM sensors by SEE are in the order of nanoamperes (nA), it is complex to be able to generate and create such a low current, despite using a very accurate signal generator. For this reason, it was decided to proceed using a 1 MΩ resistor and varying the applied voltage, to be able to obtain the injected current using Ohm's law. Furthermore, it was useful to understand how the DDC232 behaved with variation of different parameters, such as the sampling time and the range.

The Range parameter is a specific parameter of the DDC232 which allows to vary the dimensions of the feedback capacity of the integrator. The size of the digital signal output from the DDC232 was therefore plotted as function of the applied current in nanoamperes considering 3 combinations of range and sampling time. Specifically, the range was 0, 4 and 7, while the sampling time was set to 1ms, 10ms and 100 ms. The range and sampling time parameters were varied using a web application designed specifically to manage the configuration of the Teensy® microcontroller and DDC232. Furthermore, a Python application was used to read the data of the various channels and to display the output in real time.

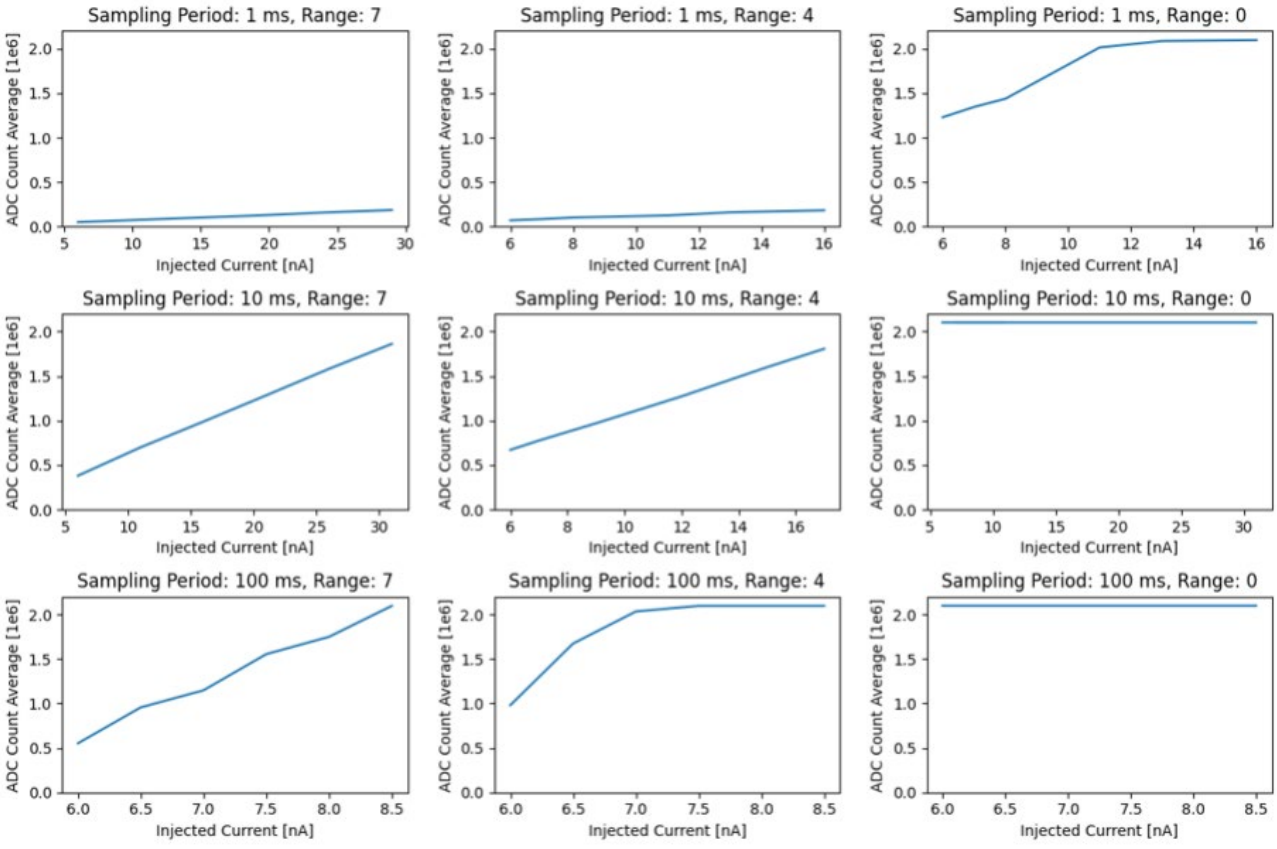

Figure 12 - Graphical visualization of ch.1 with maximum current range of 30nA

The initial test was performed in such a way so as to be able to understand the output behaviour of the DDC232 with very low current values (max 30 nA) for the different settings. The results of this test are shown in *Figure 12*. The second test was performed in order to understand how big could be

the current until the saturation was reached i.e. when the DDC232 gives in output the largest word possible (in 20 bits output configuration). The results are shown in *Figure 13*.

A graphical representation was performed for both tests showing the saturation curve. In order to have a good response, the ideal expected characteristic should be linear and space between the baseline and the saturation point, thus covering all the possible values of the output. The closest case to the ideal one is obtained for Range 7 and Sampling Period of 10 ms. Decreasing the range results in a smaller feedback capacitance for the integrator, thus having a shorter charging time for the capacitance and consequently a faster saturation for the ADC output word. The same effect can be reached increasing the sampling time. In fact, the DDC232 produces an output that is proportional to the collected charge (proportional to the input current times the acquisition time).

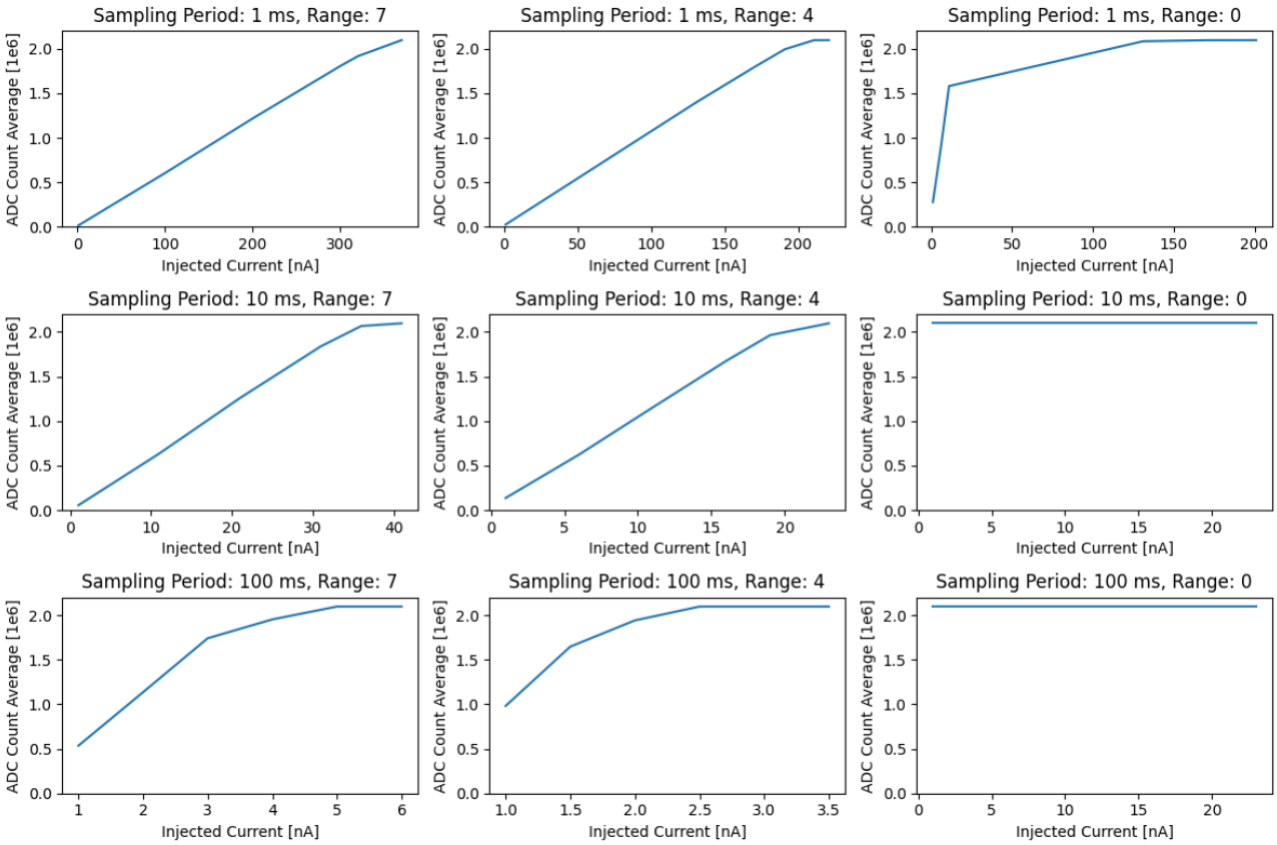

Figure 13 - Graphical visualization of ch.7 until the saturation point

The minimum appreciable current is limited by noise. When the range is maximum (range 7) and the sampling time is 1 ms, the output is too small, thus not allowing an accurate measurement due to noise. The same effect is reached with minimum range and bigger sampling time values, where the output word results to be already saturated even with 0 A of injected current. In the second case (*Figure 13*), as already mentioned, a higher current has been injected in order to reach saturation point for all cases. The most significant result is obtained for sampling period of 1 ms, where a current of more than 300 nA is needed in order to reach saturation point.

5. CONCLUSIONS

This document describes the development of the new IRRAD-BPM DAQ system for the CERN proton irradiation facility (IRRAD). The report includes the system requirements, the discussion about the design choices that were made, and the tests performed on the first protype, available at CERN in the first semester of 2023. This report is also providing a general overview of the basic functionalities of the new system as well as a first assessment of its performance. The measurements shown in section 4.2 prove that the performance of the first prototype meets the requirements set for the measurement of the new IRRAD-BPM sensors being developed for IRRAD (see section 1.1) thus confirming that the EURO-LABS MS28 has been met according to the project schedule. This development can also be used for BPM systems in other EU irradiation facilities for the monitoring particle beams.

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ANNEX: GLOSSARY

Acronym	Definition
IRRAD	CERN Proton IRRADiation Facility
BPM	Beam Profile Monitor
SEE	Secondary Electron Emission
DAQ	Data AcQuisition System