Introduction: COKA & SUMA

INFN has a large and lively community of scientists actively engaged in computational physics, working on areas such as Lattice Gauge Theories (LGT), the Physics of Complex Systems and Fluid Dynamics. These scientists use world-class computing resources, including INFN-owned computing resources, and access programmes such as PRACE.

INFN also supports these efforts with a number of projects more directly focusing on new HPC architectures, new parallel programming models, massively parallel algorithm development and optimisation; broadly speaking, the focus of these projects is to enable INFN scientists to use forthcoming Exaflops systems as efficiently as possible.

In this framework, the SUMA project, co-funded by the Italian Ministry of University and Science (MIUR), provides wide-spectrum support to the INFN computational communities, including the operation of Tier-1 HPC clusters and the funding of post-doc positions for HPC-oriented research.

The COKA project Computing on Knights and Kepler Architectures focuses on the use of accelerators in HPC general purpose computing, assessing the performance of accelerator-based systems and developing programming methodologies to effectively use all parallel features available on these processors.

The hardware targets for these tests are the recently released x86-based Intel Xeon Phi and the K20-based NVIDIA Tesla boards, as well as low-power architectures such as the CARMa boards.

The project address the performances of applications relevant in theoretical and experimental physics. This poster presents a selection of results in such diverse areas as Lattice Boltzmann methods, Monte Carlo simulations of Spin Glass systems, and LGT, as well as data-analysis and trigger computing for high energy physics experiments.

Many-core Architectures and Issues

- core parallelism: keep all 60 cores (1 reserver for OS) busy - runs 2-3 (up to) 4 threads/core is necessary to hide memory latency
- vector parallelism: enable data parallelism - enable use of 512-bit vector instructions
- Amdahl's law: accelerator device clock period is (1/n) ns - latency of PCI-E bus is

Code Portability: OpenCL

- programming framework for heterogeneous architectures: CPU + accelerators
- computing model: host code plus one or more kernels running on accelerators - kernels are executed by a set of work-items each processing an item of the data-set (data parallelism)
- work-items are grouped into work-groups, each executed by a compute-unit and processing K work-items in parallel using vector instructions - e.g. on Xeon Phi work-groups are mapped on (virtual) cores processing each up to 8 double-precisions floating-point data
- memory model identifies a hierarchy of four spaces which differ for size and access-time: private, local, global and constant memory

LQCD Pisa

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Table in [ns] run on an NVIDIA GPU using double precision

Assessment of the efficiencies and effectiveness of directive-based programming paradigms for scientific HPC applications

- Validation tool based on the Game of life 2D
- Computation enforced through a parametric Ncormp() function (Double Precision vectorization)
- Parallelization with directive based languages for GPU NVIDIA K20 (OpenACC) and MIC (openMP)
- Overlapped communication/computation with independent processing of lattice borders and internals.

Native Mode performance of complex codes based on community software used by large collaborations in computational physics

The CHROMA (http://usqcdlab.org/usqcd-directors/chroma5) application has been re-comilled on the MIC environment without any code customization; this is a key point of the MIC architecture. The timing refers to the execution of 200 sweeps on a 12x12x12x20 lattice.

The drawback of this approach is the poor performance in comparison with the execution on the computing host (2x Sandy Bridge, E5-2657W 3.10 GHz, 8 cores).

Time of execution is 412 sec on a host core while it is 7033 sec on a PHI core.

D2Q37

- Lattice size 1920x2048
- 7600 GP operations/site

References