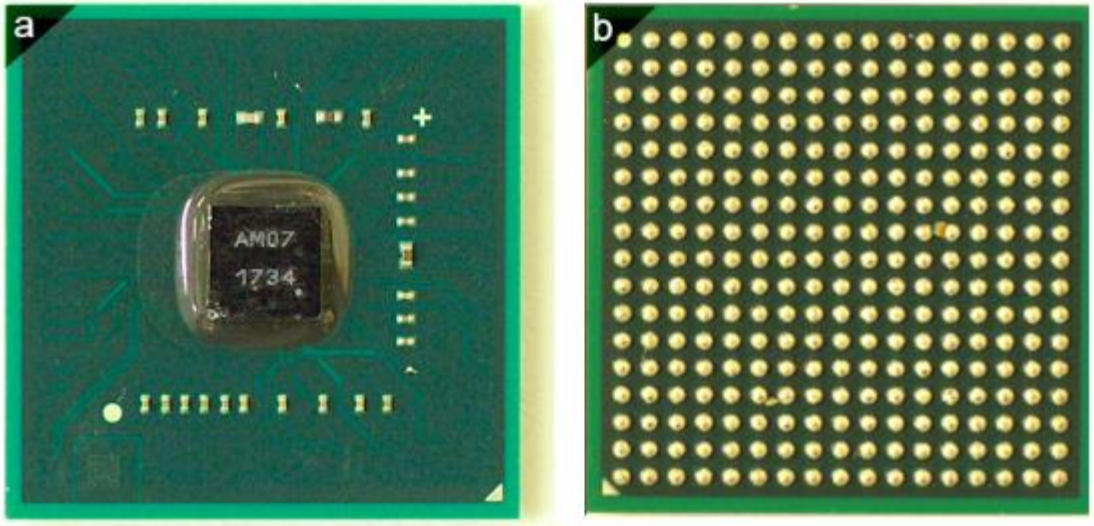
CAM - CONTENT ADDRESSABLE MEMORY



PRIORITY NUMBER:

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KEYWORDS:

CAM
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IP block

This smart Content Addressable Memory (CAM) is used for acceleration of pattern recognition processes. The technology relates on a CAM with a particular configuration which is optimized for reducing power consumption with respect to the technologies already available on the market.

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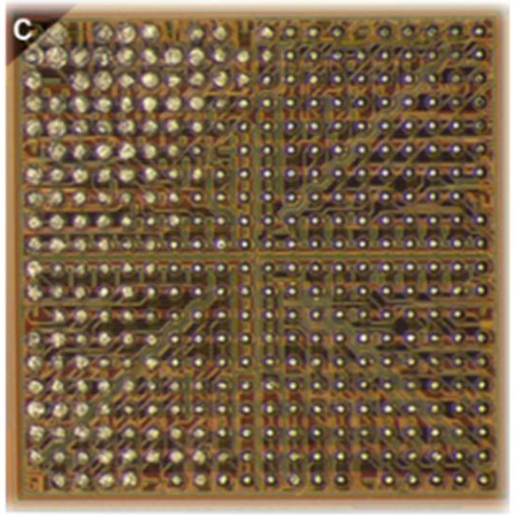

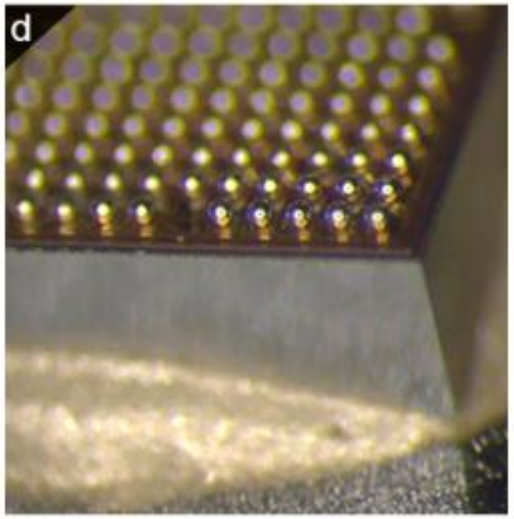

DESCRIPTION :

The CAM architecture has been properly designed to reduce the length of bit lines and consequently to cut the energy consumption related to the data flow along them. Thanks to a *matching* circuit it is possible to reduce consumption during the search phase. If one of the bits in a word is not matching, the corresponding cell sends a *kill* signal to the cascaded cell to inhibit further switching. Thanks to this feature, the designed CAM array requires less than 0.4 fJ/bit per comparison in High Power Computing (HPC) technologies and less than 0.2 fJ/bit for High Power Low-leakage technologies. This CAM cell has been designed in two variants, exploiting 28 nm CMOS technology and using a fully-CMOS approach. A prototype containing this memory has been fabricated and it has proven to be functional (up to 400 MHz) confirming power consumption expectations.

ADVANTAGES:

- Accelerated pattern recognition processes;
- Strong reduction power dissipation for a given problem with respect to FPGA or GPU;
- Easy to integrate as IP-block in ASIC projects.

APPLICATIONS:

Acceleration of pattern recognition problems for these applications:

- Images;
- DNA sequencies;
- Biomedical data.