

# THE DATA ACQUISITION SYSTEM FOR THE OBELIX CENTRAL DETECTOR

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### Abstract

The data acquisition system developed for the central detector of the OBELIX experiment at the Low Energy Antiproton Ring (LEAR) at CERN is described. The system is based on a VME multiprocessor that formats, collects and makes a rough online analysis of the events digitized by high speed (100 MHz) Flash-ADCs. Full on-line event reconstruction is also provided.

## Introduction

Today high energy physics experiments show an ever increasing number of detector channels with more and more complex electronics. The advent of fast analog-to-digital converters together with faster and less expensive microprocessors in recent years has led to a considerable change in the readout philosophy of fast detector signals. To the signal global information, like total charge and start time, is now possible to substitute the sampling of the pulse shape and find the useful parameters by a successive accurate analysis of the digitized data. This means, however, that when many channels are used the amount of data generated increase quickly. In this scheme, to avoid recording a huge quantity of raw data, a powerful on-line readout and analysis is needed.

Due to the parallel nature of the readout a parallel multiprocessor system whose central architecture is based on the industry-standard VME/VSB bus was the appropriate solution adopted by several experiments<sup>1-5</sup>).

On the other hand, nowadays also powerful and cheaper workstations are available and permit to handle the user interface, the analysis and the graphical representation of the data.

In this context we have developed our data acquisition system, using techniques that, in our opinion, are quite general.

## The detector

The detector (Fig.1) - called Spiral Projection Chamber (SPC)<sup>6</sup>) or X-ray Drift Chamber (XDC)<sup>7</sup>) depending whether the use as charged particle or X-ray detector is emphasized - surrounds a cylindrical gas H<sub>2</sub> target at STP and is positioned along the axis of the Open Axial Field Magnet in the center of the Obelix experiment.

The detector is used as X-ray Drift Chamber to identify and measure, with good resolution, the energy of the soft X-rays (0.5-15 KeV) emitted in the atomic cascade of  $p\bar{p}$  atoms formed by stopping antiprotons in the H<sub>2</sub> target surrounded by the SPC. The SPC is used to count the multiplicity of charged particles

emitted in  $p\bar{p}$  annihilation, to measure directions and relative angles of prongs, to reconstruct accurately in three dimensions the annihilation vertex and also to veto events with antiprotons scattered too far away from the  $\bar{p}$  beam axis and entering the SPC active volume.

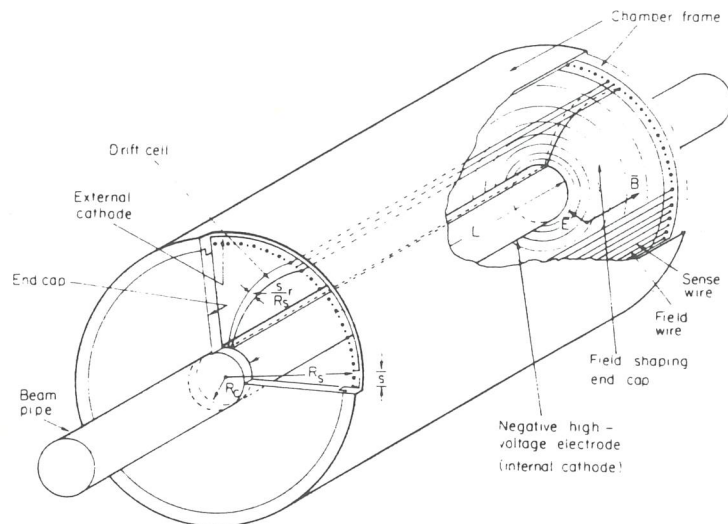


Fig. 1. Scheme of the Spiral Projection Chamber with contours of one of the drift cells.

The detector is a 90-cell cylindrical projection chamber with radial drift field. The counter gas is separated from the  $H_2$  target gas by a thin mylar tube ( $\Phi = 6 \text{ cm}$ ,  $\sim 6 \mu\text{m}$  thickness) to allow good transmission for soft X-rays. The mylar tube also acts as an internal cathode surface for the drift chamber. Primary ionization clusters are localized in three dimension by wire number  $\Phi$ , drift time ( delay of the leading edge of the associated pulse )  $t$ , and charge division  $z$ . The absorption point of a X-ray and the generation point of a sizeable cluster produced by passage of an ionizing particle are thus determined (using only the information of the anode wires), with an error  $\sigma_\phi = 1.3^\circ$ ,  $\sigma_r = 300 \mu\text{m}$ ,  $\sigma_z \sim 10 \text{ mm}$ . 90 cathode strip are wound on the inside of the external cathode surface of the chamber so that each strip crosses 85 sense wires. The strips are equipped on one side with the same front end and read out electronic of the anodes.

## The data acquisition system

To clarify the context in which the SPC Data Acquisition is implemented, a brief description of the logical scheme of the whole Obelix Data Acquisition system<sup>8,9</sup>) is given now (Fig.2).

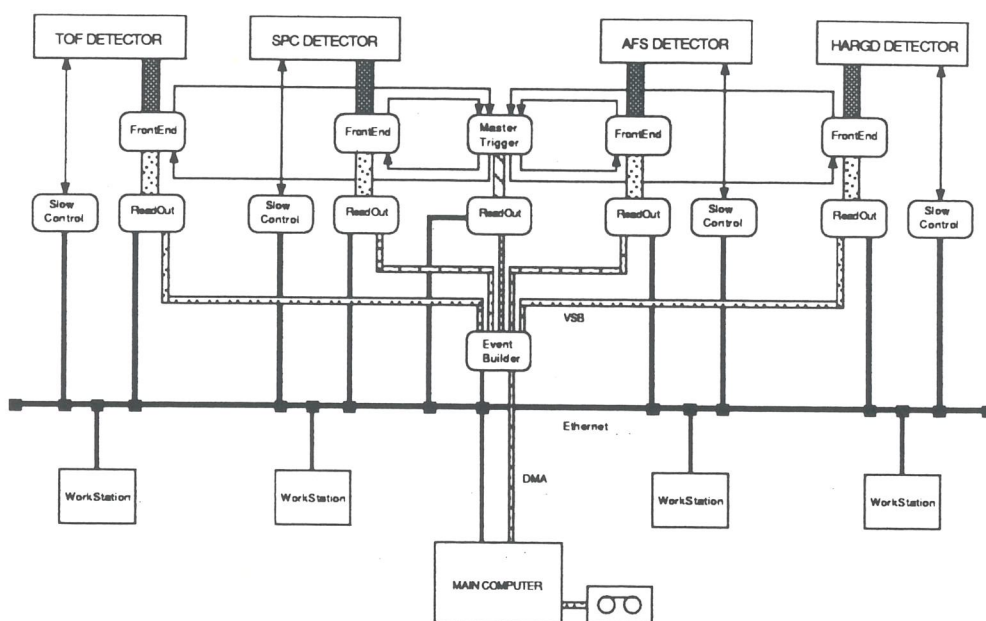


Fig.2 - The OBELUX Data Acquisition System

The experimental setup consists of four detectors. The basic idea in the system design is the achievement of a centralized control during the data taking and the possibility of working on each detector independently during the development stage and testing. Another important characteristic is that each detector data acquisition system has the same kind of architecture. The differences are due to the front end readout electronics built on different buses and the different VME levels that the complexity of apparatus needs. This permits the use of the same software and hardware environment reducing the software development efforts and allowing an easy hardware resource interchange between detectors.

All computers are linked together through Ethernet which has a bandwidth sufficient to pass commands, alarms, histograms, etc. From a logical point of view, each sub data acquisition system has the following structure:

- a *front end*, that converts the analog signals, produced by the detector, in digitized data;
- a *VME multiprocessor readout system*, that reads, filters and formats the events;
- a *VME slow control*, to setting and monitoring the detector hardware (HW, pressure, etc.);
- a *powerful workstation* as supervisor of the system, that handles the interface to the user and the graphical representation of the data.

The four detectors are synchronized by a *master trigger supervisor* and the subevents produced by the readout systems are sent, via the local bus VSB, to the *Global Event Builder* (GEB) where the complete event is assembled and sent to the *main computer* for recording and monitoring.

Fig.3 shows how this architecture as been implemented for the SPC Data Acquisition System<sup>10,11</sup>).

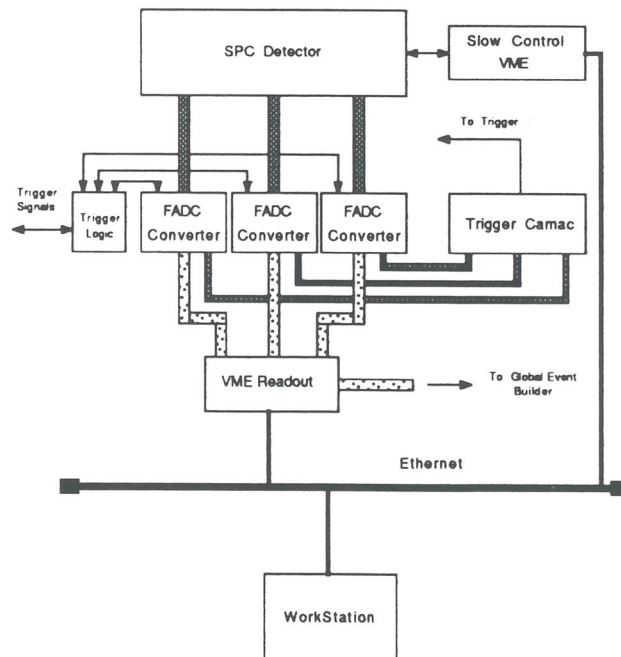


Fig.3 - The SPC Data Acquisition System

## The Front-End

As already said the detector generate 180 pulses (one for each wire end) and 90 pulses for the strips. The frontend is based on analog to digital converter Flash-ADC system, called DL300 (Fig.4)<sup>12</sup>). This consists of a specialized crate that can house up to 24 FADC boards, each with 4 FADC, a SCANNER module to make zero suppression and an INTERFACE module to the readout electronics.

As each DL300 system can house up to 96 FADC we used three DL300 crates, two for wires and one for strips. The FADC sample signals every 10 ns with a 10 bit non linear resolution. The pulse shape is recorded on a local FADC memory of 1024 bytes allowing a deep time recording of 10  $\mu$ s (Fig.5).

We use the so called *common stop mode*; in this scheme the signal is repeatedly sampled until a stop arrive. The Fig.6 display the transition state diagrams of the DL300 system and SPC trigger respectively. The sequence of the operations in the DL300 system starts with an initialization phase followed by *start-sampling* and by the generation of a *ready-signal* which enables the trigger device to send at DL300 a logic signal when an annihilation occurs (first level trigger). The *stop-sampling* is directly related to the first level trigger through a constant time delay and starts some fast online evaluations which generate the second level trigger. If the event characteristics do not match with the physical constraints a *clear-signal* restarts the *sampling-phase* and the *ready-signal* is generated again. Otherwise a *ready-readout* signal disables the trigger and starts, for each wire, a scanning and readout sequence. Finally the data are written and a new event acquisition cycle restarts.

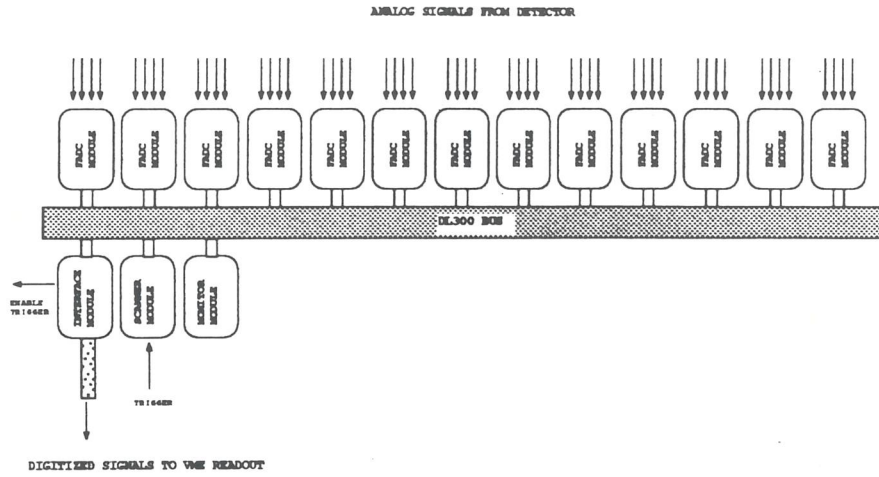


FIG. 4 - DL300 FRONT END

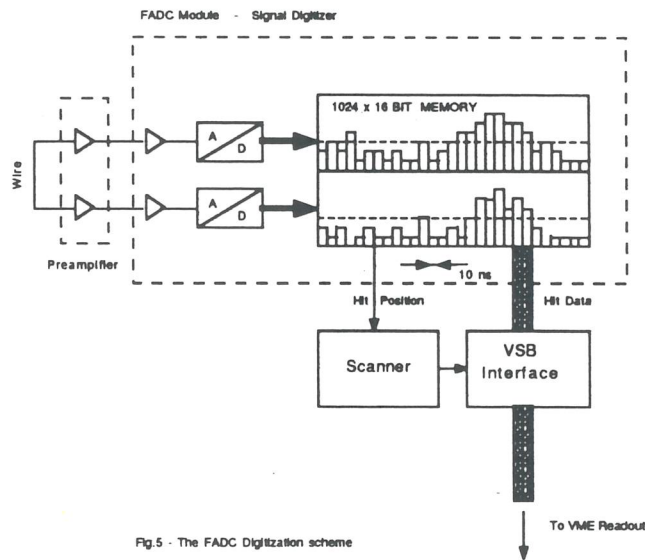


Fig.5 - The FADC Digitization scheme

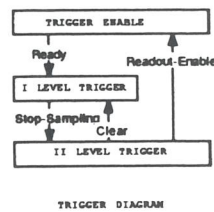
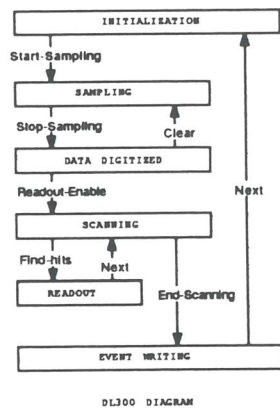


Fig.6 - State Diagrams



## The readout

### The data Flow

Fig.7 shows the analog to digital signals conversion and the data reduction after zero suppression. Since each event is divided in three parts because of the realization of frontend electronics, the three subevents are synchronized and collected together by the local event builder (LEB).

The LEB provide also the distribution of events to the consumers. The main one is the GEB, the others are the local workstation and the online analysis.

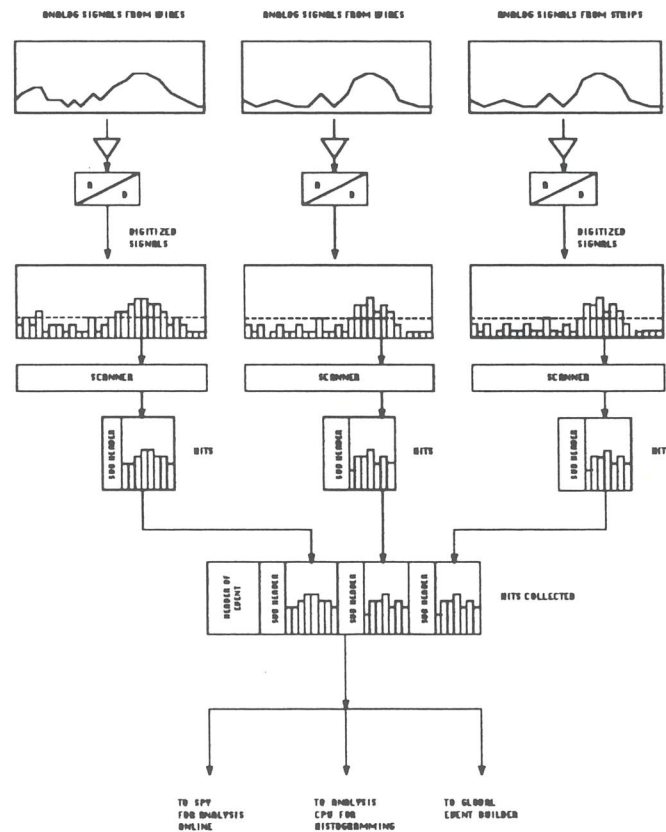


Fig.7 - The SPC data flow

## The VME readout

Fig 8 shows the hardware configuration of system. The VME bus is used for communication between the boards that have to share the resources, while VSB bus provide a local communication for CPUs that use a private resource, reducing in this way the traffic on the VME.

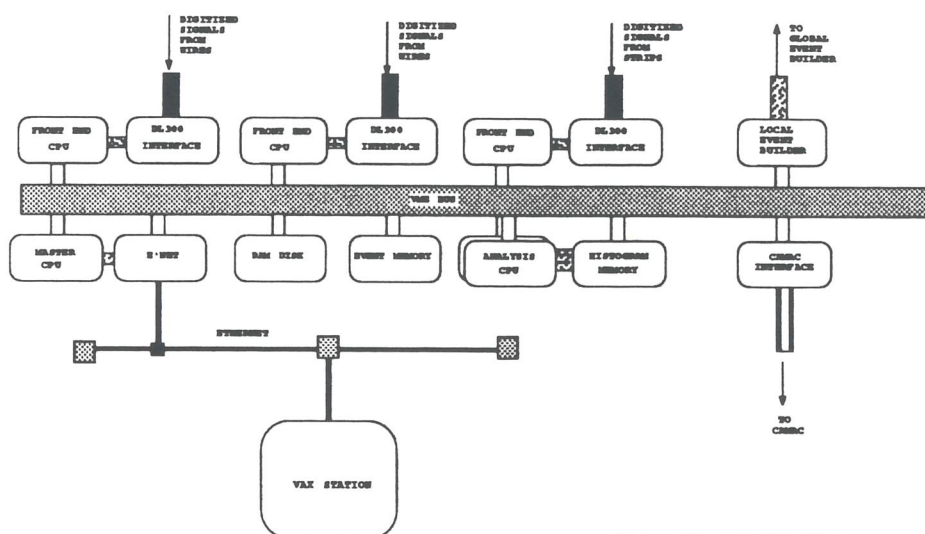


FIG.8 - THE SPC READOUT

The CPUs cards are build to our specifications by an Italian company<sup>13</sup>). They are based on Motorola 68020 microprocessor with the 68881 mathematical coprocessor. An interrupt mail box and a dual port memory are provided for use in a multiprocessor environment.

Three front end CPUs (FE CPU) controls the DL300 crates via VSB local bus, handle the readout and storage of the events on the internal dual port memory which size allows the recording of two buffers of 30 Kbytes each, that is the largest subevent size foreseen.

The local event builder CPU (LEB CPU) collects the subevents reading them from the dual ports of the FE CPUs and send the assembled event to a dual port memory of the GEB (located into another VME crate) via a differential VSB cable<sup>14</sup>), which maximum length is 50 m.

On request, a copy of the events it is also sent to *analysis* CPU (ANL CPU) and the *master* CPU (MST CPU). The task of the

ANL CPU is to make a rough online analysis and to produce histograms on a large (8 Mbytes) shared memory (Histograms Memory). In this first phase only one ANL CPU is used, we foresee to add more to adapt some procedures of the off-line analysis to this on-line environment. This will be quite natural due to the open architecture of the system.

The main task of the MST CPU is to control the Ethernet Card in order to communicate with other systems. In particular, the master handles commands arriving from the remote workstation and directs them to the slaves processors. Moreover, it can transfer events and the histograms to the workstation.

### The software

A description of the software tools has already been given elsewhere<sup>15,16</sup>). Here we give a summary.

Every VME CPU card works with a ROM based Microware OS9 operating system. A shared static memory with battery backup (seen as RAM disk by the CPUs) contains all the system modules required to boot the CPUs. A high level communication protocol (OS9/Net by Microware) has been implemented to build a CPU "network" in a single crate. Over OS9/Net we developed NetLib [] to simplify the exchange of message between CPUs.

The communication between the VME crate and the remote control station has been realized using the so called Remote Procedure Call (RPC). In our system we use the implementation realized by CERN DD<sup>17,20</sup>).

A real time version of Fortran<sup>21</sup>), C and Assembler language has been used for software development.

### **The VME slow control**

All the slow control of the detector hardware (HV, pressure, etc. of the detectors) has been allocated into a second VME crate.

We used the same hardware and the same software utils as the main VME crate. A DAC/ADC I/O card is used for the setup and the monitoring. As the system is very simple a CPU is sufficient to control the I/O board and the Ethernet Card.

Up to now the monitoring and the Setup are done using a VT200 terminal connected to the RS232 CPU serial port.

## The WorkStation

A powerful workstation based on a color DEC Vaxstation VS3100 is used to supervisors the system, to handle the interface to the user and the graphical representation of the data (Fig.9).

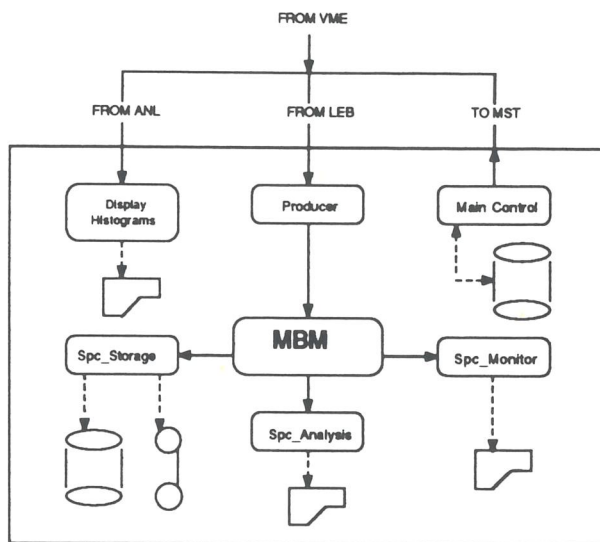


Fig.9 - The WorkStation Software structure

The VAX resident online software has been developed within the framework of MODEL, a set of modules that have been implemented by the online Computing Group of the CERN Data Division to provide an environment for data acquisition<sup>22-29</sup>).

All the programs running on the Vaxstation interact with the user via graphical menu, panel and boxes. The user interface of every program has been accomplished using three graphic tools: the Model Uman Interface [], the Model Panel, the Menu Package [] and the HGIZ [] based on GKS.

Three main procedures are directly coupled with the OS9 programs (fig x) : the MAIN CONTROL, the PRODUCER and DISPLAY HISTOGRAMS.

The MAIN CONTROL issues the main commands to the system: START, STOP and SETUP.

The DISPLAY HISTOGRAMS shows the histograms produced by the online ANL CPU.

The PRODUCER takes the events from LEB CPU. The Model Buffer Manager (MBM) has been employed to distribute the events coming from the producer to three consumers :

- Storage : to recording data on the local disk or tape;
- Monitoring : to display and print the pulses;
- Analysis : make the event reconstruction.

The principals functions provided by the analysis program are the following: in the first phase the raw data are decoded, then each pulse is associated to a spatial point (reconstruction of spatial points). The points that belong to the same track are joined together (Pattern recognition) and the track fitting give the best trajectories, then at last the vertex fitting is done to give the annihilation vertex.

### **Performances**

The system is in routine operation. The event rate range from 20 events/sec when the event size is ~ 80 Kbytes (all wires and strips hit) to 110 events/sec when the event size is ~ 2 Kbytes (2 wires and 2 strips hit). The maximum rate foreseen for the experiment is ~50 events/sec, therefore our conditions match the requirements.

We plan to speed-up the system by a 20% using an upgraded version of the CPU board based on the 68030, and adding a Digital Signal Processor (DSP) to make faster the online analysis.

## Acknowledgements

X.J. Wang (IAE, Beijing, China) contributed to the graphical system software, G. Parlati (Universita' degli Studi di Salerno) contributed to several important software applications.

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