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THE TRANSPUTER BASED GA.SP DATA ACQUISITION SYSTEM

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Contributed paper to the "REAL TIME 91" Conference, Julich - Fed. Rep. of Germany 25 - 28 June 1991
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The Transputer Based GA.SP Data Acquisition System

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Abstract

The new data acquisition for the GA.SP detector is presented. It is a distributed system based on a network of 40 T800 and T222 transputers linked to a VME system used for histogram storage. A 100 MBit/s FDDI ring connects the system to UNIX workstations used for the experiment control, histogram display and second level data analysis.

I. INTRODUCTION

A data acquisition system has been designed for the GA.SP gamma spectrometer [1]. The main aim of the detector is the search of complex structures in high spin excited levels of nuclei like superdeformed bands and hyperdeformed signatures. GA.SP consists of an array of 40 large volume Ge-suppressed (70-80% efficiency) and a multiplicity filter of 80 BGO detectors. It can operate either stand-alone or in coincidence with the recoil mass spectrometer [2] in operation at "Laboratori Nazionali di Legnaro" (LNL).

Simulations of the apparatus show an event rate of 25-35 Kevent/s and so it can be estimated that a typical experiment will gather ~10^9 events per run, corresponding to a data volume of about 10^2 Gbytes.

Off-line analysis of this huge quantity of data could be a serious problem for the production of physical results, in terms of computing power and time required. Moreover the capability to obtain quantitative results during experiments has been shown [3] to be of extreme importance for measurement economy.

Keeping this problem in mind, the GA.SP data acquisition system has been designed with the aim to move typical off-line operations (like detector recalibration, event consistency check, full event sorting, etc.) into an on-line environment. This design strategy allows to perform a real-time data reduction, but it requires a large on-line computing power.

Modern data acquisition systems, both for nuclear and high energy physics, are usually distributed systems where both hardware and software are specialized, according to the different functions to be performed. As some procedures require intensive calculation, a cost effective parallel structure is embedded on the system.

The topology of this "number crunching" is generally simple as the events to be processed are intrinsically not correlated. For the GA.SP data a pipeline structrure with high parallelization level is the most suitable.

We have chosen transputers since they can well reproduce that topology and good multiprocessing software is available. Although the single processing element is not competitive, in terms of speed, with the new generation of RISC and CISC processors, the hardware and software design of a transputer multiprocessor system is simple, efficient and effective. Moreover, a new and faster transputers family will be soon on the market.

Therefore a large (40 nodes) transputer network (T-Net) has been designed. The net is coupled to the VME environment that is used to handle large histograms and to bridge the T-Net with a fast local area network, where UNIX workstations monitor and control the experiment. Specially designed electronics interfaces T-Net with the detector front-end electronics and with the VME bus. A large memory, with autoincrement capability, has been realized to speed up the histogramming operation.

As the GA.SP spectrometer is a multiusers experimental facility, standard tools and "user friendly" software have to be provided. UNIX operating system and X-Window Motif have been chosen for workstations and VME environment. As the T-Net programming would require expertise in Occam language, a new language compiler (NEO) [4], producing Occam code, has been developed. NEO is a C like language oriented to nuclear physics data processing. It includes typical statements for data filtering and sorting and provides the structure to organize the transputer network.

II. GENERAL LAYOUT

The detector information (about 200 channels) is digitized by the front-end electronics. After zero suppression for the under threshold inputs, the data are transferred to the processing system by a 16 bit ECL bus (compatible with the FERA protocol). The processing steps are shown in fig. 2.1 where the system is logically described by a data flows diagram.

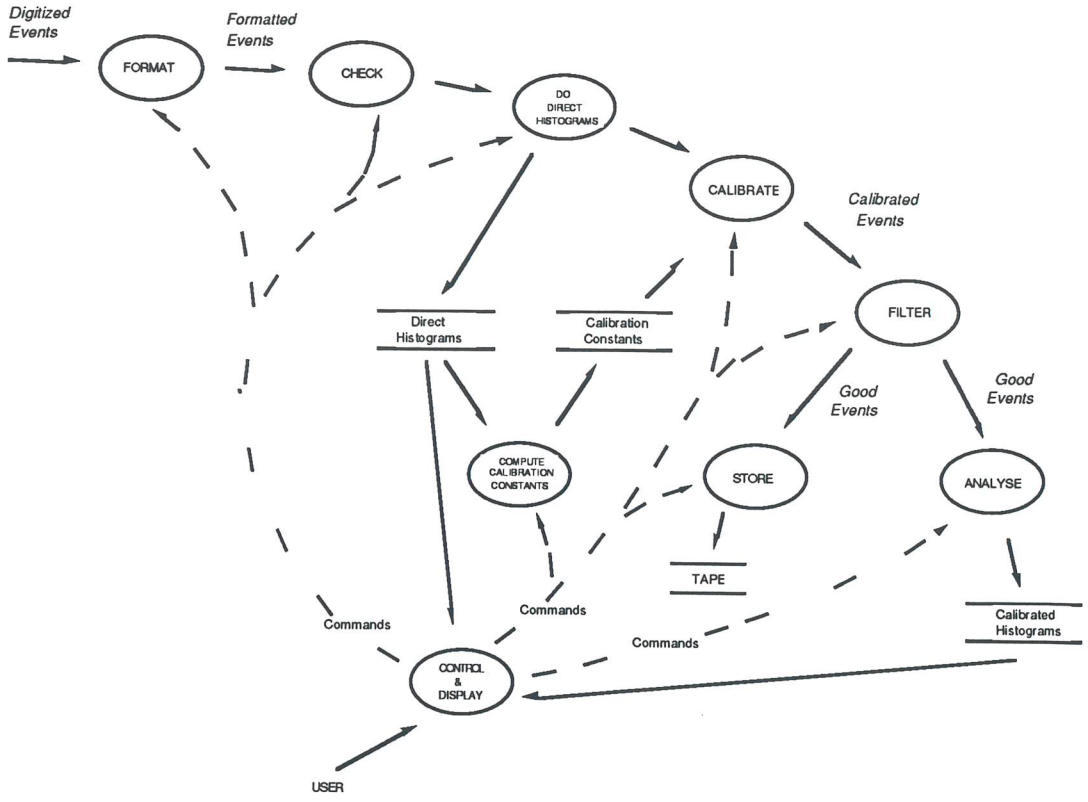

Fig. 2.1 GA.SP data acquisition flow diagram

The incoming event is first formatted (*Format*) reorganizing the event parameters in a proper way for further processing and several checks on the hardware consistency are performed. The event type and its physical consistency is then checked (*Check*) in order to skip spurious or incomplete events. On-line calibration procedures (*Calibrate*) equalizes the detector channel gains and corrects the gain shifts and other distortions (ballistic effect, doppler shift, etc.). The calibration constants are computed (*Compute Calibration Constants)* analysing the histograms produced by the raw event parameters (*Do Direct Histograms*) and stored in the Direct Histogram data base. The estimated dimension of the database is 20 Mbyte (each Ge detector has one monodimensional histogram and one bidimensional histogram).

Filter procedure selects the event on user defined conditions basis (one dimension gates, banana gates, etc.). *Store* saves the data on the mass storage, while in parallel *Analyse* performs the data sorting. The last procedure updates the histograms of the Calibrated Histograms data base. The total amount of memory for building mono and bidimensional histograms (4096 x 4096) is 200 Mbyte.

The databases are implemented in RAM memory since a high histogramming speed (10^6 updating/s) is required.

The *Control & Display* procedure controls the system sending commands to all processes and receiving the corresponding status. It interacts with the histogram databases and provides for their graphical representation.

III. ARCHITECTURE

The procedures of the logical scheme of fig. 2.1 have been grouped in the functional scheme of fig. 3.1.

The most time consuming tasks are put together in order to study the feasibility of an "event processing accelerator".The inherent parallelism of the data to be processed moves naturally to design a parallel computing system.

In the field of nuclear physics several multiprocessor bus based systems has been built (most of them in the VME framework [5,6]. A VME based "accelerator" for GA.SP detector would be feasible with commercially available cards and could provide the required performances. Good operating systems are on the market (also with a good multiprocessor extension) but they are usually available only for a given target CPU card. Their porting on a different hardware platform is possible but it requires a lot of time and expertise. Moreover, the improving in overall performance of the system becomes less and less significant as the number of processors becomes large. This is mainly due to bandwidth limits but also to technical aspects of the software.

A large number of processors is more effectively connected if communication between them is "message passing" instead of "memory shared" based. Using this approach, it is possible to built a network that scales in performance according to the number of processors, provided that communication time is a small fraction of processing time.

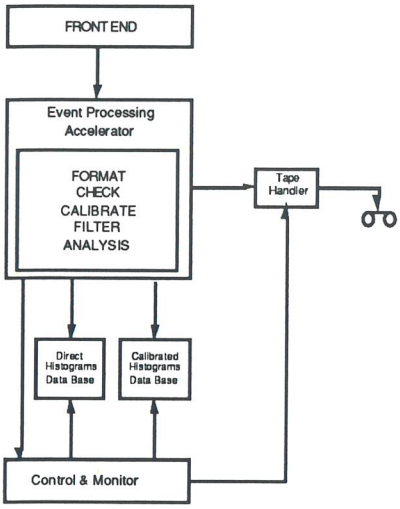

Fig. 3.1 GA.SP Data Acquisition functional scheme

For these reasons we have designed a network based on transputers processors.

The transputer is a family of programmable devices that have been developed by INMOS as elementary blocks for building large processors array. It combines a RISC processor, a memory and four bidirectional serial communication links on one chip. The current floating point version (T800 - 30 MHz) has a peak instruction rate of 30 MIPS and 4.3 MFlops, 4 Kbytes of on-chip RAM and 2 Mbyte per second link speed. The RISC architecture and the on-chip hardware scheduler allows context switching to be very fast (few microseconds), supporting efficient implementation of concurrent program execution on a single transputer. The links support DMA communication between programs running on separate transputers. The transputers implement the Occam model of concurrency, the Occam program language having been developed in parallel with the transputer hardware. Occam is a high level language based on the theoretical model of "Communicating Sequential Processes" [7]. Communication between processes is effected by point to point "channels" which may connect processes on the same or different transputers.

The topology of the designed tranputer network (T-Net) will be described in the next paragraph. Here we want to stress that, although it would be possible to design the whole data acquisition system with transputers, the best choice is to select hardware and software platforms according to specific functionality. This means for instance,that *Control&Monitor* procedures are best performed with UNIX workstations, equipped with X-Window based human interface and adequate graphics tools (GKS, PHIGS, etc.). The data bases that require, in total, a RAM memory of the order of 200 Mbyte have to be accessible to the T-Net and to the workstations. Modern workstations can be provided with so large a bulk memory, but the heavy T-Net access would slow down workstation operations. On the other hand interfacing problems would arise implementing the memory on the transputer frame. It has been therefore chosen to interpose a VME system between workstations and T-Net and the data base memory has been realized using VME cards.Fig. 3.2 reports the block diagram of the on-line system architecture.

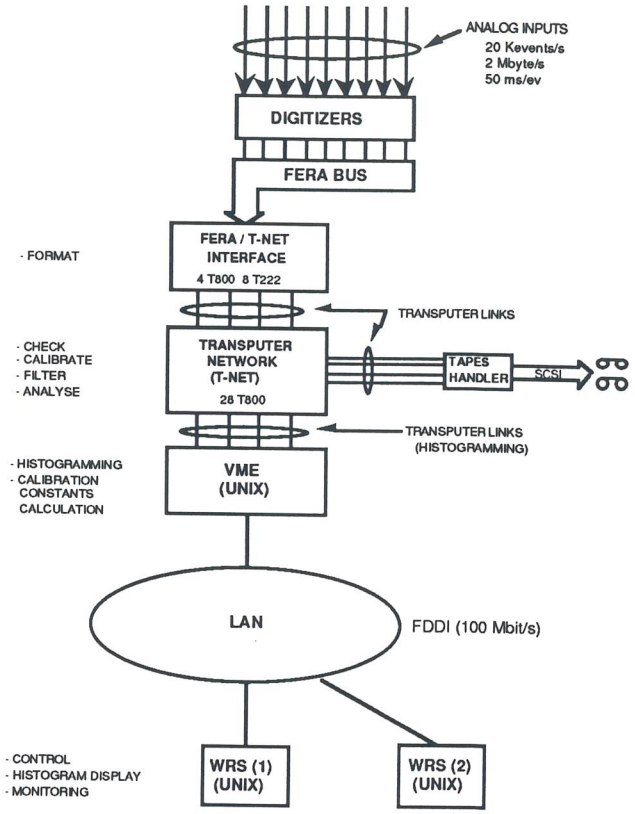

Fig. 3.2 GA.SP Data Acquisition block diagram.

The communication between the front-end electronics and the transputer framework is provided by the Fera/T-Net interface [8] that also performs the *Format* operation, using the on-board T222 transputers. T-Net performs all the time critical procedures and a tape handler, also transputer based, controls the data storage. The histogramming memory is made up of 4 x 64 Mbyte [9] VME memory cards with autoincrement capability.The T-Net addresses the memory through a special link adaptor VME card [10].

A VME CPU card (25 MHz Motorola 68030), performs calibration constant calculation (*Compute Calibration Constants)* and a fast LAN (based on FDDI protocol) links the T-Net/VME system to the workstations that control and monitor the experiment. Fig. 3.3 gives a sketch of the VME system layout.

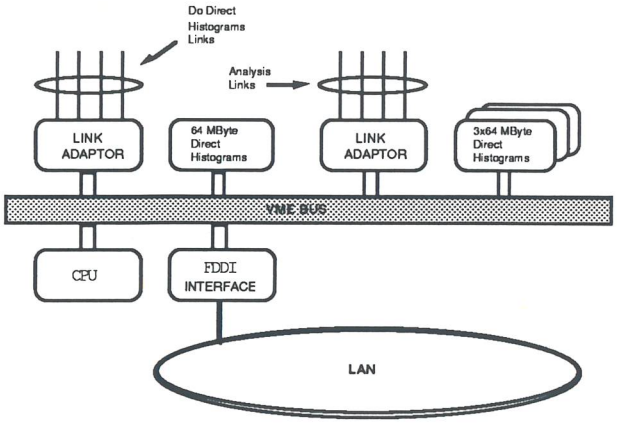

Fig. 3.3 VME system layout.

4.1 The Transputer Network (T-Net)

The average processing time for the procedures *Format*, *Check*, *Calibrate*, *Filter* and *Analysis*, has been measured using a chain of five transputers (25 MHz T800) working in pipeline. It is respectively: 350, 200, 50, 200 and 150 μs.Of course, this simple structure doesn't match the detector time requirements (50 μs/event).Two different topologies have been then considered.

The first is a set of processor farms (one per procedure) in pipeline connection as reported in fig. 3.4.

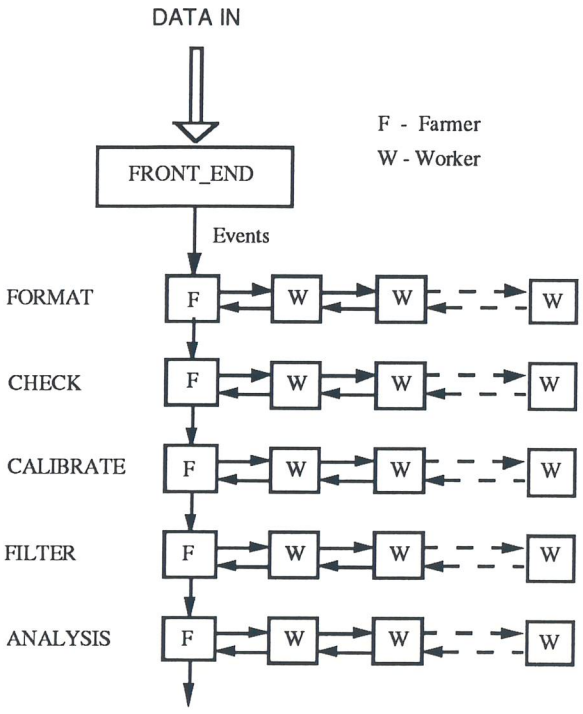

Fig. 3.4 Farmer T-Net Topology

This configuration has the advantage of having only one data input point and therefore a simple interfacing with FERA bus. The computing power is easily adjustable adding transputers where necessary. The bottleneck of this topology is the link speed. Although transputers can sustain an effective 1.7 Mbyte/s link speed, communication protocol slows down the data moving along the chain so that we are fairly far from our target of 2 Mbyte/s. Moreover the fault tolerance is poor: if a link or a transputer farmer fails, the whole network locks.

In the topology of fig. 3.5, data processing is done by a few transputer chains working in parallel. Every chain performs the processing steps in pipeline on the incoming events that are circularly distributed between the chains.

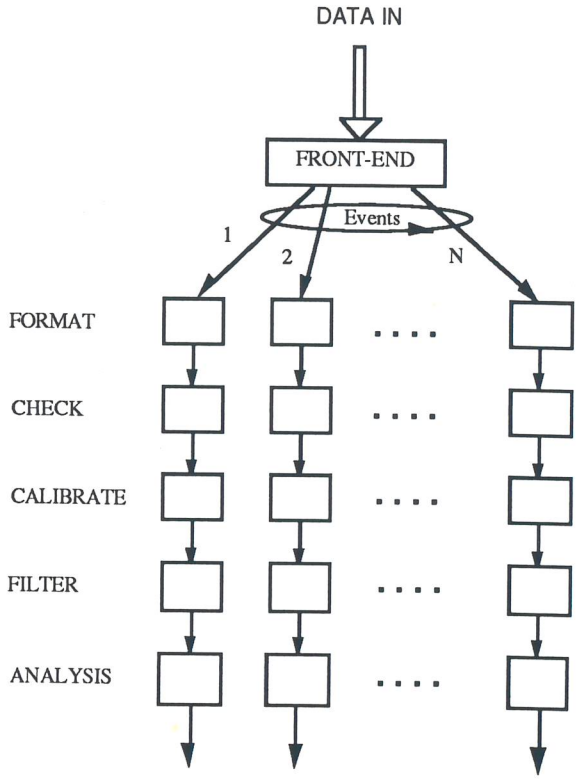

Fig. 3.5 Chains T-Net Topology

The throughput of the system is proportional to the number of activated chains and a good fault tolerance is achieved, since a chain fault reduces the system performance, but doesn't lock the system. One disadvantage of this configuration is that event distribution has to be provided by the FERA/T-Net interface by ,for speed constrains, an hardware multiplexer.The design of the interface is therefore quite complex.

The second topology has been chosen for its large flexibility.

Four chains meet the time requirement of the detector, provided two transputers per chain are dedicated to the *Format* operation, that is the most time consuming. If more computing power is necessary (e.g. for particularly heavy filter

operation) every chain can be easily farmed like in fig. 3.4. Since the input data rate is reduced by a factor of four, the link speed doesn't limit the farm performance. Fig. 3.6 describes the components of a chain.

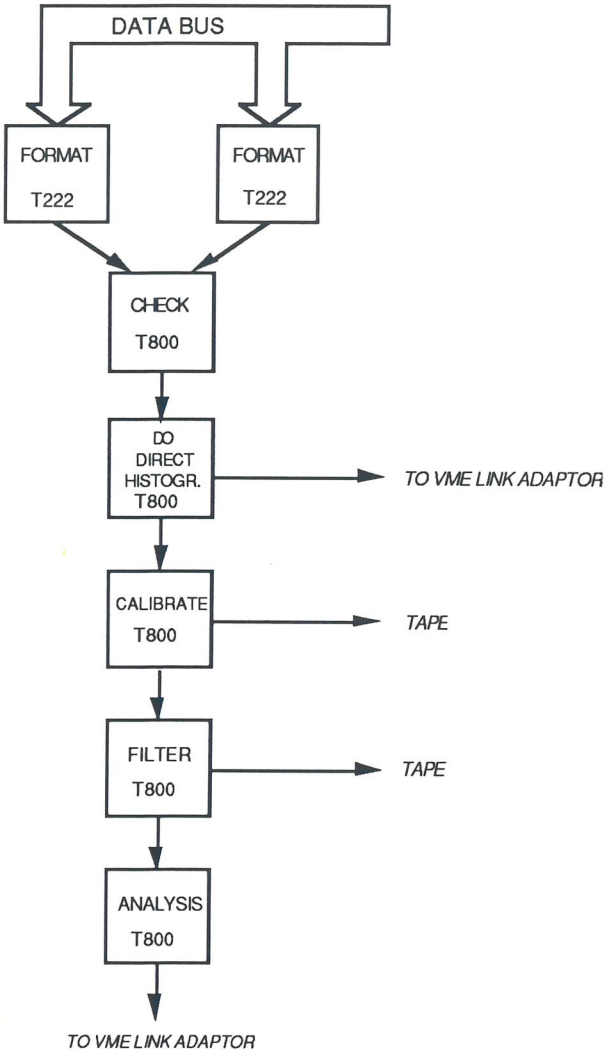

Fig. 3.6 Chain Components

IV. THE HARDWARE DEVELOPMENTS

Commercially available cards have been used where possible but special design hardware has been required for the FERA/T-Net interface, the VME histogramming memory card and the VME link adaptor card. A brief description is reported.

A. The VME histogramming memory card.

The memory is a VME/VSB slave with data broadcast and block transfer capability.

A built-in autoincrement function has been implemented on the memory in order to provide a fast histogramming.

A processor (or more generally a bus master) increments a histogram channel driving a special code on the address modifier (AM) lines and starting a dummy read operation on the memory location address of the channel to be incremented. The AM code triggers the autoincrement function and the corresponding memory cell is automatically incremented. Both word and longword increments are provided. Operation is done in one bus cycle that is, in the worst case, 550 ns.

The memory is realized with a motherboard of 16 MByte and three plug-in cards of 16 MByte each. The possible configurations are therefore 16, 32, 48 and 64 MByte. 4 MBit chips have been used but 1 Mbit chips can be also mounted on the card allowing sizes of 4, 8, 12 and 16 MByte.

Being the memory size very large, a built-in fast erase function has been provided. The whole memory can be cleared in 1.8 seconds.

B. The FERA/T-Net Interface.

The Fig. 4.1 reports the interface block diagram.

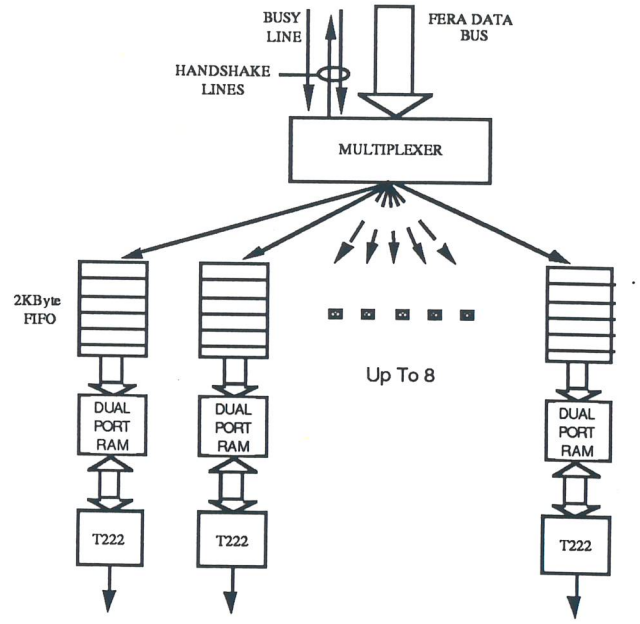

Fig. 4.1 Block diagram of FERA/T-Net Interface.

The incoming events (read from the FERA bus) are distributed, following a round robin scheme, to the FIFOs of the chains. When a complete event is stored in a FIFO, it is moved (in the DMA mode) to the local dual-port memory of a T222 transputer and an interrupt request is sent to the processor (driving its EVENT line). The read-out software is then activated and the memory is free to perform another DMA operation on the next event. The BUSY line of the FERA bus is used to switch the events from one chain to the other.

For mechanical and modularity reasons, the interface is splitted in 4 CAMAC cards each one serving two chains.

The first phase of the project has been carried out using, for the T222 read-out transputers, commercially available cards. The prototype is now in operation. A second phase of the project will provide the on board T222s.

C. The Transputer link adaptors VME card.

To interface the T-Net with the histogramming memory,a VME card has been realized .The addresses of the memory loctions to be incremented are serially provided by the four output links of the net.This information is parallelized in order to obtain the proper VME address and a AM generator gives the right Address Modifier code.

Fig. 4.2 shows the block diagram of the card that also provides a full VME bus MASTER logic. The card is fully tested and debugged. The card can sunstain up to 250 x 10^3 histogram increments per second.

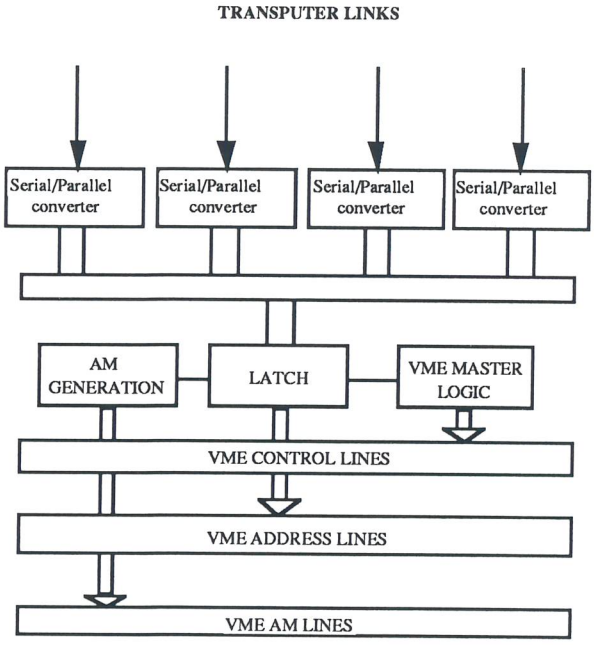

Fig. 4.2 Block diagram of transputer link adaptor.

V. CONCLUSIONS

A prototype of 16 transputers (2 chains) is in operation at LNL. Tests have been made using a BGO detector and a γ ray source . The event rate, measured with a realistic analysis is 12 Kevents/s. A 4 chains system will, therefore, give a global performance matching the requirements.

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